ABSTRACT OF THE DISCLOSURE

A floating gate of a nonvolatile memory cell is formed from two conductive layers (410.1, 410.2). A dielectric (210) in substrate isolation regions and the first of the two conductive layers providing the floating gates (410.1) are formed so that the dielectric has an exposed sidewall. At least the top portion of the sidewall is exposed. Then some of the dielectric is removed from the exposed portions of the dielectric sidewalls to laterally recess the sidewalls. Then the second conductive layer (410.2) for the floating gates is formed. The recessed sidewalls of the dielectric allow the second conductive layer to expand laterally, thus increasing the capacitive coupling between the floating and control gates and improving the gate coupling ratio.